WHAT IS CLAIMED IS:

1. A method of exporting from a data processor a plurality of parameter values of an emulation parameter that is indicative of a data processing operation performed by the data processor, comprising:

detecting a condition wherein a first portion of a first said parameter value is identical to a corresponding portion of a second said parameter value; and

in response to detection of said condition, outputting, via terminals of the data processor, said second parameter value and only a remainder portion of said first parameter value other than said first portion of said first parameter value.

2. The method of Claim 1, wherein said outputting step includes outputting information indicative of said condition.

3. The method of Claim 2, wherein said condition information includes a compression map including a plurality of bits which respectively correspond to a plurality of portions of the emulation parameter and whose values indicate which of the respectively corresponding portions of the first parameter value are identical to corresponding portions of the second parameter value.

4. The method of Claim 1, including detecting a further condition wherein a first group of bits within the remainder portion of the first parameter value all have the same bit value and a predetermined bit within a second group of bits in the remainder

portion has a bit value equal to the bit value of the bits of the first group, and, in response to detection of said further condition, said outputting step including outputting from the data processor via the terminals thereof only the second group of bits of the remainder portion without outputting the first group of bits.

5. The method of Claim 1, wherein said outputting step includes outputting said second parameter value and said remainder portion in a sequence of output information, and wherein said second parameter value precedes said remainder portion in said sequence.

6. The method of Claim 5, wherein said outputting step includes outputting in said sequence information indicative of said condition.

7. The method of Claim 6, wherein said condition information precedes said remainder portion in said sequence.

8. The method of Claim 7, wherein said second parameter value precedes said condition information in said sequence.

9. The method of Claim 6, wherein said second parameter value precedes said condition information in said sequence.

10. The method of Claim 1, wherein said emulation parameter is program counter contents.

11. The method of Claim 1, wherein said emulation parameter is a memory address.

12. The method of Claim 1, wherein said emulation parameter is memory data.

13. The method of Claim 1, wherein each of said first and second parameter values includes a plurality of bytes, said first portion includes a byte of said first parameter value, said remainder portion includes another byte of said first parameter value, and said corresponding portion includes a byte of said second parameter value.

14. The method of Claim 13, wherein said first portion includes a plurality of further bytes of said first parameter value, and said corresponding portion includes a plurality of further bytes of said second parameter value.

15. The method of Claim 1, including receiving said remainder portion and said second parameter value externally of the data processor, and recreating said first portion based on said second parameter value.

16. The method of Claim 1, wherein said outputting step includes outputting information indicative of said condition, and further including receiving said remainder portion and said second parameter value and said condition information externally of the data processor, and recreating said first portion based on said condition information and said second parameter value.

17. An integrated circuit, comprising:

a data processor for performing data processing operations;

a plurality of terminals for outputting information;

an apparatus for exporting from said integrated circuit a plurality of parameter values of an emulation parameter that is indicative of a data processing operation performed by said data processor, said apparatus including an input coupled to said data processor for receiving said parameter values, and an information generator coupled to said input for detecting a condition wherein a first portion of a first said parameter value is identical to a corresponding portion of a second said parameter value, said information generator operable for providing information which indicates that said condition has been detected; and

said apparatus further including a compression determiner coupled to said information generator and said input and said terminals, said compression determiner responsive to said condition information for outputting via said terminals said second parameter value and only a remainder portion of said first parameter value other than said first portion of said first parameter value.

18. The integrated circuit of Claim 17, wherein said compression determiner is further operable for outputting said condition information via said terminals.

19. The integrated circuit of Claim 18, wherein said condition information includes a compression map including a plurality of bits which respectively correspond to a plurality of portions of the emulation parameter and whose values indicate which of the respectively corresponding portions of the first parameter value are identical to corresponding portions of the second parameter value.

20. The integrated circuit of Claim 17, wherein said apparatus further includes an evaluator coupled to said input for detecting a further condition wherein a first group of bits within said remainder portion of said first parameter value all have the same bit value and a predetermined bit within a second group of bits in the remainder portion has a bit value equal to the bit value of the bits of said first group, said evaluator operable for providing information which indicates that said further condition has been detected, said compression determiner coupled to said evaluator and responsive to said further condition information for outputting via said terminals only said second group of bits of said remainder portion without outputting said first group of bits.

21. The integrated circuit of Claim 17, wherein said apparatus includes an information stream generator coupled between said compression determiner and said

terminals for outputting said second parameter value and said remainder portion in a sequence of output information, and wherein said second parameter value precedes said remainder portion in said sequence.

22. The integrated circuit of Claim 21, wherein said information stream generator is operable for outputting said condition information in said sequence.

23. The integrated circuit of Claim 22, wherein said condition information precedes said remainder portion in said sequence.

24. The integrated circuit of Claim 23, wherein said second parameter value precedes said condition information in said sequence.

25. The integrated circuit of Claim 22, wherein said second parameter value precedes said condition information in said sequence.

26. The integrated circuit of Claim 21, wherein said information stream generator includes a packet stream generator.

27. The integrated circuit of Claim 17, wherein said emulation parameter is one of program counter contents, a memory address and memory data.

28. A data processing system, comprising:

an integrated circuit, including a data processor for performing data processing operations;

an emulation controller coupled to said integrated circuit for controlling emulation operation of said data processor;

said integrated circuit including an apparatus coupled between said data processor and said emulation controller for exporting from said integrated circuit a plurality of parameter values of an emulation parameter that is indicative of a data processing operation performed by said data processor, said apparatus including an input coupled to said data processor for receiving said parameter values, and an information generator coupled to said input for detecting a condition wherein a first portion of a first said parameter value is identical to a corresponding portion of a second said parameter value, said information generator operable for providing information which indicates that said condition has been detected; and

said integrated circuit including a plurality of terminals coupled to said emulation controller for outputting information to said emulation controller, and said apparatus further including a compression determiner coupled to said information generator and said input and said terminals, said compression determiner responsive to said condition information for outputting to said emulation controller, via said terminals, said second parameter value and only a remainder portion of said first parameter value other than said first portion of said first parameter value.

29. The system of Claim 28, including a man/machine interface coupled to said emulation controller for permitting a user to communicate with said emulation controller.

30. The system of Claim 29, wherein said man/machine interface includes one of a visual interface and a tactile interface.